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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,591	10/24/2001	James R. Kohn	1376.687US1	8554

21186 7590 02/12/2004

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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2186	5

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/045,591	Applicant(s) KOHN ET AL.	
	Examiner Denise Tran	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-22 are presented for examination.

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 8-11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In particular, claims 8-11, computer instruction set claimed as computer listing per se, i.e., the descriptions of the computer instruction set are not physical "things." They are neither the computer components nor statutory processes. The claims 8-11, for a computer instruction set, without the computer-readable medium needed to realize the computer instruction set's functionality , should be treated as nonstatutory functional descriptive material.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Faanes et al., U.S. Patent No. 6,496,902 (hereinafter Faanes).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claims 1, 8, 12, Faanes teaches the use of maintaining a cache memory in a computer system having a first processor, a first memory, and at least a first cache between the first processor and the first memory (e.g. figure 1), comprising:

Performing a first memory access to the first memory by the first processor (e.g. col. 10, lines 49-67);

Storing a first cache line from the first memory into the first cache (e.g. col. 10, lines 49-67 and figure 1, element 120 of CPU 0);

Performing an instruction that enables a cache-invalidate function to be performed by the first processor upon execution of a resource-synchronization instruction (i.e., field 181 is not set) (e.g. col. 12, lines 30-45);

Performing the resource-synchronization instruction, wherein at least the first cache line is invalidated in the first cache (e.g. col. 12, lines 30-45);

Performing a second memory access to the first memory by the first processor (i.e., subsequent to the first access) (e.g. col. 10, lines 49-67);

Storing a second cache line from the first memory into the first cache (i.e., subsequent to the first cache line) (e.g. col. 10, lines 49-67 and figure 1, element 120 of CPU 0);

Performing an instruction that disables the cache-invalidate function from being performed by the first processor upon execution of the resource-synchronization instruction (i.e., field 181 is set) (e.g. col. 12, lines 30-45);

Performing the resource-synchronization instruction, wherein at least the second cache line is not invalidated in the first cache (e.g. col. 12, lines 30-45).

As per claims 2, 16, 21, Faanes teaches the use of a second processor and at least a second cache between the second processor and the first memory (e.g. figure 1, element 120 of CPU1), comprising:

Performing a third memory access to the first memory by the second processor (e.g. col. 10, lines 49-67);

Storing a third cache line from the memory into the second cache (e.g. col. 10, lines 49-67);

Performing the instruction that enables the cache-invalidate function to be performed by the second processor upon execution of the resource-synchronization instruction (e.g. col. 12, lines 30-45);

Performing the resource-synchronization instruction, wherein at least the third cache line is invalidated in the second cache, and wherein no data in the first cache is invalidated (e.g. col. 12, lines 30-45);

Performing a fourth memory access to the first memory by the second processor (e.g. col. 10, lines 49-67);

Storing a fourth cache line from the first memory into the second cache (e.g. col. 10, lines 49-67);

Performing the instruction that disables the cache-invalidate function from being performed by the second processor upon execution of the resource-synchronization instruction (e.g. col. 12, lines 30-45);

Performing the resource-synchronization instruction, wherein at least the fourth cache line is not invalidated in the first cache (e.g. col. 12, lines 30-45).

As per claims 3, 5, 9, 13, 17, Faanes teaches the use of the resource-synchronization instruction is a test-and-set instruction (e.g. col. 12, lines 30-45).

As per claims 4, 6, 9, 10, 11, 14, 15, 18, 19, 22, Faanes teaches the use of the instruction that enables the cache-invalidate function is an enable-test-and-set-invalidate instruction, and the instruction that disables the cache invalidate function is a disable-test-and-set-invalidate instruction (e.g. col. 12, lines 30-45); the instruction that enables the cache-invalidate function is an resource-synchronization instruction-invalidate instruction, and the instruction that disables the cache invalidate function is a disable- resource-synchronization instruction -invalidate instruction (e.g. col. 12, lines 30-45).

As per claim 7, 20, Faanes shows the entire cache is invalidated (e.g. col. 12, lines 30-45).

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Brandt et al, "The Benchmarker's Guide for CRAY SV1 Systems", Cray Inc., 7/20/2000, pages 1-39 shows test and set and avoiding cache invalidation; and

b) Faanes et al. (US 2002/0144061 A1) show disabling a cache-invalidate function.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday and an alternated Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for central Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Denise Tran

D.T
February 8, 2004